CLAIMS

1. A pulse-width controller comprising:

a first pulse generator coupled to receive a clock signal and configured to extend a first pulse width to provide a first pulse-width adjusted signal;

a second pulse generator coupled to receive an inverted version of the clock signal and configured to extend a second pulse width to provide a second pulse-width adjusted signal;

control signal generator logic coupled to receive the first adjusted pulse-width signal and the second adjusted pulse-width signal and configured to generate control signals in response to the first adjusted pulse-width signal and the second adjusted pulse-width signal;

differential logic coupled to receive the clock signal, the inverted version of the clock signal, the control signals, the first adjusted pulse-width signal, an inverted version of the first adjusted pulse-width signal and the second adjusted pulse-width signal;

the differential logic configured to provide the clock signal and the inverted version of the clock signal to a differential output of the differential logic responsive to the control signals, the clock signal and the inverted version of the clock signal;

the differential logic further configured to provide the first adjusted pulse-width signal to the differential output responsive to the first adjusted pulse-width signal and the inverted version of the first adjusted pulse-width signal; and

the differential logic further configured to provide the second adjusted pulse-width signal to the differential output responsive to the second adjusted pulse-width signal.

2. The pulse-width controller, according to claim 1, wherein the first pulse width is a high-time pulse width that is extended to fall within a first target range.

3. The pulse-width controller, according to claim 2, wherein the second pulse width is a low-time pulse width that is extended to fall within a second target range.

4. The pulse-width controller, according to claim 3, wherein the differential output is adjusted to approximately a 50%-50% duty cycle.

5. The pulse-width controller, according to claim 1, wherein the clock signal and the inverted version of the clock signal are a differential output of an oscillator control circuit.

6. The pulse-width controller, according to claim 5 wherein the differential output comprises a positive side clock signal and a negative side clock signal each of which is a differential logic signal.

7. The pulse-width controller, according to claim 6, wherein the differential logic signal of the positive side clock signal and the differential logic signal of the negative side clock signal are Differential Cascode Voltage Switch Logic signals.

8. The pulse-width controller, according to claim 7, wherein the control signals are Complementary Metal-Oxide-Semiconductor logic signals.

9. The pulse-width controller, according to claim 7, wherein the first adjusted pulse-width signal, the inverted version of the first adjusted pulse-width signal, and the second adjusted pulse-width signal are Complementary Metal-Oxide-Semiconductor logic signals.

10. The pulse-width controller, according to claim 1, wherein the first adjusted pulse-width signal is a high-time adjusted pulse-width signal, wherein the second adjusted pulse-width signal is a low-time adjusted pulse width signal, and wherein the high-time adjusted pulse-width signal and the low-time

adjusted pulse width signal are respective inputs to a NAND gate to provide a control signal of the control signals.

11. The pulse-width controller, according to claim 10, wherein the control signal is inverted to provide another control signal of the control signals.

12. A system for an integrated circuit for providing a phase-aligned, duty-cycle adjusted signal, comprising:

a pulse-width controller including:

a first pulse generator coupled to receive a clock signal and configured to extend a first pulse width to provide a first pulse-width adjusted signal;

a second pulse generator coupled to receive an inverted version of the clock signal and configured to extend a second pulse width to provide a second pulse-width adjusted signal;

control signal generator logic coupled to receive the first adjusted pulse-width signal and the second adjusted pulse-width signal and configured to generate control signals in response to the first adjusted pulse-width signal and the second adjusted pulse-width signal;

first differential logic coupled to receive the clock signal, the inverted version of the clock signal, the control signals, the first adjusted pulse-width signal, an inverted version of the first adjusted pulse-width signal and the second adjusted pulse-width signal;

the first differential logic configured to provide the clock signal and the inverted version of the clock signal to a first differential output of the first differential logic responsive to the control signals, the clock signal and the inverted version of the clock signal;

the first differential logic further configured to provide the first adjusted pulse-width signal to the first differential output responsive to the first adjusted pulse-width signal and the inverted version of the first adjusted pulse-width signal;

the first differential logic further configured to provide the second adjusted pulse-width signal to the first differential output responsive to the second adjusted pulse-width signal; and

an oscillator controller coupled to provide the clock signal and the inverted version of the clock signal as a differential input to the pulse-width controller.

13. The system, according to claim 12, further comprising delay line circuitry coupled to receive the first differential output of the pulse-width controller.

14. The system, according to claim 13, wherein the first differential output comprises a positive side clock signal and a negative side clock signal.

15. The system, according to claim 14, wherein the delay line circuitry is configured to provide an oscillator signal and an inverted version of the oscillator signal; and wherein the oscillator controller is coupled to receive the oscillator signal and the inverted version of the oscillator signal.

16. The system, according to claim 15, wherein the phase controller comprises:

second differential logic for receiving a differential reference input, the differential reference input associated with a reference signal;

the second differential logic for receiving a differential oscillator input, the differential oscillator input associated with the oscillator signal, the reference signal and the oscillator signal having different frequencies;

the second differential logic configured to provide a second differential output at least partially responsive to at least one of the reference signal and the oscillator signal;

control logic for receiving second control signals and configured to selectively couple and decouple respective portions of the second differential logic responsive to the

second control signals;

the control logic configured to put the second differential logic in one of three states in response to the second control signals; and

the three states including a state for shifting by the second differential logic an edge of the reference signal to the second differential output for a hard-phase alignment.

17. The system, according to claim 16, wherein the integrated circuit comprises a digital clock manager circuit including the subsystem.

18. The system, according to claim 17, wherein the integrated circuit is a programmable logic device.

19. The system, according to claim 18, wherein the integrated circuit is a field programmable gate array.

20. The subsystem, according to claim 16, wherein the phase controller comprises:

second differential logic for receiving a differential reference input, the differential reference input associated with a reference signal;

the second differential logic for receiving a differential oscillator input, the differential oscillator input associated with the oscillator signal, the reference signal and the oscillator signal having different frequencies;

the second differential logic configured to provide a second differential output at least partially responsive to at least one of the reference signal and the oscillator signal;

the second differential logic configured to provide a combinational circuit in an oscillator alignment state and to provide a sequential circuit in a hard-phase alignment state;

control logic for receiving second control signals and configured to selectively couple and decouple respective portions of the second differential logic responsive to the second control signals; and

the control logic in part to selectively alternate between putting the second differential logic in the oscillator alignment state and in the hard-phase alignment state responsive to the second control signals.

21. The subsystem, according to claim 20, wherein the integrated circuit comprises a digital clock manager circuit including the subsystem.

22. The subsystem, according to claim 21, wherein the integrated circuit is a field programmable gate array.

23. An pulse-width controller for an integrated circuit, comprising:

a first means for receiving a clock signal configured to extend a high-time pulse width to provide a first pulse-width adjusted signal;

a second means for receiving an inverted version of the clock signal configured to extend a low-time pulse width to provide a second pulse-width adjusted signal;

control means for receiving the first adjusted pulse-width signal and the second adjusted pulse-width signal configured to generate control signals in response to the first adjusted pulse-width signal and the second adjusted pulse-width signal;

a third means coupled to receive the clock signal, the inverted version of the clock signal, the control signals, the first adjusted pulse-width signal and the second adjusted pulse-width signal;

the third means configured to provide the clock signal and the inverted version of the clock signal to a differential output of the third means responsive to the control signals, the clock signal and the inverted version of the clock signal;

the third means further configured to provide the first adjusted pulse-width signal to the differential output responsive to the first adjusted pulse-width signal and the inverted version of the first adjusted pulse-width signal; and

the third means further configured to provide the second

adjusted pulse-width signal to the differential output responsive to the second adjusted pulse-width signal;

wherein the differential output is duty cycle adjusted.

24. A method for pulse-width control, comprising:

receiving a clock signal;

generating first pulses responsive to the clock signal with an extended high-time pulse width to provide a first pulse-width adjusted signal;

receiving an inverted version of the clock signal;

generating second pulses responsive to the inverted version of the clock signal with an extended low-time pulse width to provide a second pulse-width adjusted signal;

generating control signals responsive to the first adjusted pulse-width signal and the second adjusted pulse-width signal;

shifting the first adjusted pulse-width signal to a differential output of differential logic responsive to assertion of the first adjusted pulse-width signal;

shifting the clock signal and the inverted version of the clock signal to the differential output responsive to the control signals; and

shifting the second adjusted pulse-width signal to the differential output responsive to assertion of the second adjusted pulse-width signal and an inverted version of the second adjusted pulse-width signal.